Claims

We claim:

1. A multi-layered interconnect structure, comprising:

a thermally conductive layer including first and second opposing surfaces;

a first and a second dielectric layer positioned on the first and the second opposing surfaces, respectively, of the thermally conductive layer;

first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively;

a first electrically conductive layer within said first dielectric layer;

a second electrically conductive layer within said first dielectric layer and positioned between said first electrically conductive layer and said thermally conductive layer, wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors;

a plated through hole through the multi-layered interconnect structure electrically connected to at least one member of said first plurality of electrically conductive members, to at least one of said first plurality of shielded signal conductors, and to at least one member of said second plurality of electrically conductive members; and

a third dielectric layer positioned on said first dielectric layer and on portions of said first plurality of electrically conductive members, said third dielectric layer substantially overlying said plated through hole, and wherein said third dielectric layer includes a first high density interconnect layer for providing an electrical path from a first electronic device to the first

plurality of shielded signal conductors..

2. The multi-layered interconnect structure of claim 1, wherein said third dielectric layer includes a resin comprising an allylated polyphenylene ether.

3. The multi-layered interconnect structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the thermally conductive layer is between about one third and about two thirds of an overall CTE of the multi-layered interconnect structure.

4. The multi-layered interconnect structure of claim 1, further comprising a plated blind via in the third dielectric layer, wherein the plated blind via is conductively coupled to the at least one member of said first plurality of electrically conductive members.

5. The multi-layered interconnect structure of claim 4, further comprising a first electronic device conductively coupled to the plated blind via.

6. The multi-layered interconnect structure of claim 5, wherein the first electronic device is selected from the group consisting of the semiconductor chip and the circuitized substrate.

7. The multi-layered interconnect structure of claim 1, further comprising:

a third electrically conductive layer within said second dielectric layer;

a fourth electrically conductive layer within said second dielectric layer and positioned

between said third electrically conductive layer and said thermally conductive layer, wherein said fourth electrically conductive layer comprises a second plurality of shielded signal conductors; and

a fourth dielectric layer positioned on said second dielectric layer and on portions of said second plurality of electrically conductive members, said fourth dielectric layer substantially overlying said plated through hole, wherein said fourth dielectric layer includes a second high density interconnect layer for providing an electrical path from a second electronic device to the second plurality of shielded signal conductors.

8. The multi-layered interconnect structure of claim 7, wherein said fourth dielectric layer includes a resin comprising an allylated polyphenylene ether.

9. The multi-layered interconnect structure of claim 7, further comprising:

a first plated blind via in the third dielectric layer, wherein the first plated blind via is conductively coupled to the at least one member of said first plurality of electrically conductive members; and

a second plated blind via in the fourth dielectric layer, wherein the second plated blind via is conductively coupled to the at least one member of said second plurality of electrically conductive members.

10. The multi-layered interconnect structure of claim 9, further comprising:

a first solder connection conductively coupled to the first plated blind via;

a second solder connection conductively coupled to the second plated blind via;

a first electronic device conductively coupled by the first solder connection to the first plated blind via; and

a second electronic device conductively coupled by the second solder connection to the second plated blind via.

11. The multi-layered interconnect structure of claim 10, wherein the first electronic device is a semiconductor chip, and wherein second electronic device is the circuitized substrate.

12. The multi-layered interconnect structure of claim 10, wherein the multi-layered interconnect structure has an overall CTE that will not cause failure of: the first solder connection, the second solder connection, and interconnection within the multi-layered interconnect structure.

13. The multi-layered interconnect structure of claim 10, wherein the difference between an overall CTE of the multi-layered interconnect structure and a CTE of the first electronic device is between about 40% and about 60% of the difference between a CTE of the second electronic device and the CTE of the first electronic device.

14. A method of making a multi-layered interconnect structure, comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

forming first and second dielectric layers on said first and second opposing surfaces, respectively, of said thermally conductive layer;

forming first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively;

forming a first electrically conductive layer within said first dielectric layer;

forming a second electrically conductive layer within said first dielectric layer and positioned between said first electrically conductive layer and said thermally conductive layer, wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors;

forming a plated through hole through the multi-layered interconnect structure electrically connected to at least one member of said first plurality of electrically conductive members, to at least one of said first plurality of shielded signal conductors, and to at least one member of said second plurality of electrically conductive members; and

forming a third dielectric layer on said first dielectric layer and on portions of said first plurality of electrically conductive members, said third dielectric layer substantially overlying said plated through hole, and wherein said third dielectric layer includes a first high density interconnect layer for providing an electrical path from a first electronic device to the first plurality of shielded signal conductors.

15. The method of claim 14, wherein a coefficient of thermal expansion (CTE) of the thermally conductive layer is between about one third and about two thirds of an overall CTE of the multi-layered interconnect structure.

16. The method of claim 14, wherein said third dielectric layer includes a resin comprising an allylated polyphenylene ether.

17. The method of claim 16, wherein the step of forming a third dielectric layer comprises:

providing a sheet that includes a layer of the resin on a rough surface of a metal foil;

placing the sheet on said first dielectric layer and on said first plurality of electrically conductive members, wherein the metal foil is exposed;

pressurizing the multi-layered interconnect structure at a pressure, elevated temperature, and for a time duration necessary for the resin to cure and for the layer of the resin to adhesively laminate to said first dielectric layer and to said first plurality of electrically conductive members; and

removing the metal foil, leaving an exposed rough surface of the layer of resin that is complementary to the rough surface of the first metal foil.

18. The method of claim 17, wherein the metal foil includes copper.

19. The method of claim 17, wherein the removing step includes etching away the metal foil.

20. The method of claim 17, further comprising oxidizing exposed surfaces of the first plurality of electrically conductive members, before the step of placing the sheet.

21. The method of claim 17, wherein the pressure is between about 1000 psi and about 2000 psi, the temperature is between about 180°C and about 210°C, and the time exceeds about 90 minutes.

22. The method of claim 14, further comprising forming a plated blind via in the third dielectric layer, wherein a the plated blind via is conductively coupled to the at least one member of said first plurality of electrically conductive members.

23. The method of claim 22, further comprising conductively coupling an electronic device to the plated blind via.

24. The method of claim 23, wherein the electronic device is selected from the group consisting of a semiconductor chip and a circuitized substrate.

25. The method of claim 23, wherein the electronic device is the semiconductor chip, and wherein the step of coupling the semiconductor chip to the plated blind via includes:

applying a first solder paste onto the plated blind via; and

reflowing the first solder paste to form a solder connection;

applying a second solder paste onto the solder connection;

positioning a contact member of the semiconductor chip on the solder connection; and

reflowing the second solder paste to conductively couple the semiconductor chip to the plated blind via.

26. The method of claim 14, further comprising:

forming a third electrically conductive layer within said second dielectric layer;

forming a fourth electrically conductive layer within said second dielectric layer and positioned between said third electrically conductive layer and said thermally conductive layer, wherein said fourth electrically conductive layer comprises a second plurality of shielded signal conductors; and

forming a fourth dielectric layer on said second dielectric layer and on portions of said second plurality of electrically conductive members, said fourth dielectric layer substantially overlying said plated through hole, wherein said fourth dielectric layer includes a second high density interconnect layer for providing an electrical path from a second electronic device to the second plurality of shielded signal conductors.

27. The method of claim 26, wherein said fourth dielectric layer includes a resin comprising an allylated polyphenylene ether.

28. The method of claim 27, wherein the steps of forming a third dielectric layer and a fourth dielectric layer comprise:

providing a first sheet that includes a first layer of the resin on a rough surface of a first

metal foil;

providing a second sheet that includes a second layer of the resin on a rough surface of a second metal foil;

placing the first sheet on said first dielectric layer and on said first plurality of electrically conductive members, wherein the first metal foil is exposed;

placing the second sheet on said second dielectric layer and on said second plurality of electrically conductive members, wherein the second metal foil is exposed;

pressurizing the multi-layered interconnect structure at a pressure, elevated temperature, and for a time duration necessary for the resin to cure, for the first layer of the resin to adhesively laminate to said first dielectric layer and to said first plurality of electrically conductive members, and for the second layer of the resin to adhesively laminate to said second dielectric layer and to said second plurality of electrically conductive members;

removing the first metal foil, leaving an exposed rough surface of the first layer of resin that is complementary to the rough surface of the first metal foil; and

removing the second metal foil, leaving an exposed rough surface of the second layer of resin that is complementary to the rough surface of the second metal foil.

29. The method of claim 28, further comprising:

oxidizing exposed surfaces of the first plurality of electrically conductive members, before the step of placing the first sheet; and

oxidizing exposed surfaces of the second plurality of electrically conductive members, before the step of placing the second sheet.

30. The method of claim 28, wherein the pressure is between about 1000 psi and about 2000 psi, the temperature is between about 180 °C and about 210 °C, and the time exceeds about 90 minutes.

31. The method of claim 26, further comprising:

forming a first plated blind via in the third dielectric layer, wherein the first plated blind via is conductively coupled to the at least one member of said first plurality of electrically conductive members; and

forming a second plated blind via in the fourth dielectric layer, wherein the second plated blind via is conductively coupled to the at least one member of said second plurality of electrically conductive members.

32. The method of claim 31, further comprising:

forming a first solder connection conductively coupled to the first plated blind via;

forming a second solder connection conductively coupled to the second plated blind via;

conductively coupling a first electronic device, by the first solder connection, to the first plated blind via; and

conductively coupling a second electronic device, by the second solder connection, to the second plated blind via.

33. The method of claim 32, wherein the first electronic device is a semiconductor chip, and wherein second electronic device is a circuitized substrate.

34. The method of claim 32, wherein the multi-layered interconnect structure has an overall CTE that prevents failure of: the first solder connection, the second solder connection, and interconnection within the multi-layered interconnect structure.

35. The method of claim 32, wherein the difference between an overall CTE of the multi-layered interconnect structure and a CTE of the first electronic device is between about 40% and about 60% of the difference between a CTE of the second electronic device and the CTE of the first electronic device.